



PATENT

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March 3, 2004

Date

Ayesha J. Shaikh

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/779,305

Confirmation No. : Not Yet Assigned

Applicant : Philip Neaves

Filed : February 13, 2004

Attorney Docket No.: 501340.02

Art Unit : Not Yet Assigned

Customer No. : 27,076

Examiner : Not Yet Assigned

Title : STRUCTURE AND METHOD FOR FORMING A CAPACITIVELY COUPLED CHIP-TO-CHIP SIGNALING INTERFACE

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449. Copies of the cited foreign patent and non-patent literature references, as required under 37 C.F.R. § 1.98(a)(2), are enclosed. Copies of the cited U.S. patents and U.S. patent application publications will not be submitted herewith in accordance with the waiver by the Office of the requirement under 37 C.F.R. § 1.98(a)(2)(i) for U.S. national patent applications filed after June 30, 2003. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicant's duty to disclose all information he is aware of which is believed relevant to the examination of the above-identified application, applicant believes that his invention is patentable.



Please acknowledge receipt of this Supplemental Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

DORSEY & WHITNEY LLP

Steven H. Arterberry
Registration No. 46,314

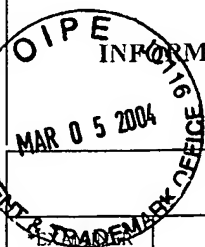
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Enclosures:

- Postcard
- Form PTO-1449
- Cited References (9)

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FORM PTO-1449
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
501340.02APPLICATION NO.
10/779,305

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

APPLICANT(S)
Philip NeavesFILING DATE
February 13, 2004GROUP ART UNIT
Not Yet Assigned

U.S. PATENT DOCUMENTS

INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
1	AA	6,188,232 B1	02/13/01	Akram et al.	324	755	
	AB	6,285,201 B1	09/04/01	Farnworth et al.	324	755	
	AC	6,357,025 B1	03/12/02	Tuttle	714	724	
	AD	6,368,930 B1	04/09/02	Enquist	438	320	
	AE	6,396,292 B2	05/28/02	Hembree et al.	324	755	
	AF	6,407,566 B1	06/18/02	Brunelle et al.	324	758	
	AG	6,490,188 B2	12/03/02	Nuxoll et al.	365	63	
	AH	6,563,133 B1	05/13/03	Tong	257	52	
	AI	6,563,299 B1	05/13/03	Van Horn et al.	324	158.1	
	AJ	6,620,638 B1	09/16/03	Farrar	438	14	
	AK	6,625,073 B1	09/23/03	Beffa	365	201	
	AL	2001/0054908 A1	12/27/01	Farnworth et al.	324	755	
	AM						
	AN						
	AO						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AP	0 277 764 A3	01/27/88	EP			X	
	AQ	0 492 806 A3	11/26/91	EP			X	
	AR	0 805 356 A3	04/22/98	EP			X	
	AS	2 353 401 A	02/21/01	GB			X	
	AT	2 353 402 A	02/21/01	GB			X	
	AU						X	
	AV						X	

EXAMINER

DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 501340.02	APPLICATION NO. 10/779,305
INFORMATION DISCLOSURE STATEMENT <i>(Use several sheets if necessary)</i>				APPLICANT(S) Philip Neaves	
				FILING DATE February 13, 2004	GROUP ART UNIT Not Yet Assigned
OTHER PRIOR ART <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>					
	AW	"International Technology Roadmap for Semiconductors", Assembly and Packaging, 2001, pp. 1-21.			
	AX	Karnezos, M. et al., "System in a Package (SiP) Benefits and Technical Issues", in <i>Proceedings of APEX</i> , San Diego, California, 2002, 7 pages.			
	AY	Mick, S. et al., "4Gbps High-Density AC Coupled Interconnection", Department of Electrical and Computer Engineering North Carolina State University, IEEE Custom Integrated Circuits Conference, May 12-16, 2002, pp. 133-140.			
	AZ	"Rapidly Advancing System-in-Package Fabrication Technology", Vol. 20, No.3, 2002, pp. 3-11.			
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EXAMINER				DATE CONSIDERED	
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